

## **ABSTRACT OF THE DISCLOSURE**

NAND type non-volatile ferroelectric memory cell and non-volatile ferroelectric memory of the same, in which numbers of access to a main cell and a reference cell are made the same, to maintain bitline induced voltages by the reference cell and by the main cell constant, for improving operation characteristics, minimizing a layout area, and permits a high density device integration, the memory cell including an N number of transistors connected in series, a bitline having an input terminal of a first transistor and an output terminal of (N)th transistor among the N number of transistors connected thereto, wordlines respectively connected to gates of the transistors except the (N)th transistor, a WEC signal line connected to a gate of the (N)th transistor and adapted to have an enable signal applied thereto only in a write or re-store mode, and ferroelectric capacitors respectively connected both to the wordlines and output terminals of the transistors.